THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte TATSUO HIGUCHI
and
NAOKI HAMANAKA

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Appeal No. 1996-2195
Application 08/120,911[1]

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ON BRIEF

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Before HAIRSTON, FLEMING and HECKER, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

[1] Application for patent filed September 15, 1993.

This is a decision on appeal from the final rejection of claims 39 through 44, 46 through 74, 77 and 78.

Claims 1

through 38 have been cancelled. On February 1, 1995, Appellants filed an amendment after final which was entered into the record. The amendment cancelled claims 52 and 77 and amended claim 39. Therefore, claims 39 through 44, 46 through 51, 53 through 74 and 78 are properly before us for our consideration on appeal.

The present invention relates to a processor with cache memory used in a multiprocessor system. In particular, the invention relates to a processor having a main cache and a receive cache memory. The receive cache memory is for receiving data from other processors in the network. The processor is able to read data from either the main cache or the receive cache in parallel.

Independent claim 39 is reproduced as follows:

39. A processor for a multiprocessor system connected to a network, comprising:

an instruction processor for executing instructions;

a local memory for holding instructions to be executed by the instruction processor and data to be processed thereby, and an access controller for controlling access to said local memory;

a main cache for holding part of data held by said local memory and a main cache controller connected to said main cache and instruction processor, and said access controller for controlling said main cache; and

a sending unit connected to said main cache for sending data on the network and a receiving unit for receiving data from the network;

a receive cache and a receive cache controller connected to said receive cache, said receive unit and said instruction processor and said access controller for controlling the receive cache so that said receive cache temporarily stores data received by the receiving unit which is to be stored in said local memory;

said main cache controller responding to a memory write request provided by said instruction processor for first data to be written into the local memory, so as to write said write data into said main cache,

said main cache controller not writing said received data into said main cache and said receive cache controller not writing said first data requested by said memory write request into said receive cache;

said main cache controller and said receive cache controller both further responding to a common memory read request initiated by said instruction processor unit for second data held in said local memory so as to read the second data requested by the read request from one cache which holds

said second data among said main cache and said receive cache; and

said main cache controller further responding to a memory read request provided by said sending unit for send data so as to supply the send data from the main cache to the sending unit.

The Examiner relies on the following references:

Watkins et al. (Watkins)	5,247,648	Sept. 21, 1993 (filed Apr. 30, 1992)
Segers	5,249,282	Sept. 28, 1993 (filed Nov. 21, 1990)

Claims 39 through 44, 46 through 51, 53 through 74 and 78 stand rejected under 35 U.S.C. § 103 as being unpatentable over Watkins in view of Segers.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs[2] and answer for the respective details thereof.

[2] Appellants filed an appeal brief on July 3, 1995. Appellants filed a reply brief on November 22, 1995. The Examiner mailed a communication on January 23, 1996 stating that the reply brief has been considered and no further response by the Examiner is deemed necessary.

OPINION

We will not sustain the rejection of claims 39 through 44, 46 through 51, 53 through 74 and 78 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness,

the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 519 U.S. 822 (1996) ***citing W. L. Gore & Assoc., Inc. v. Garlock,***

Inc., 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied,*** 469 U.S. 851 (1984).

Appellants argue on page 11 of the brief that Watkins' CPU can only use a central cache with respect to either reading or writing data, but cannot use the I/O cache. Appellants point out that Watkins' CPU uses the I/O cache only for specific pur-poses including executing the flush cycle, pointing to column 21, line 66, to column 22, line 14. Appellants point out that the use of the central cache and the I/O cache by the CPU results from the basic concept of operation disclosed by Watkins wherein the I/O cache is used for holding data which has been written from outside the processor by each I/O device that is to be written into the system memory.

Appellants argue that their invention operates differently in that the processor of their invention has a main cache and a receive cache wherein the instruction processor uses

only the main cache with respect to writing the data and uses both caches for reading the data. Thus, the CPU is allowed to access receive data held in the receive cache directly without reading the data from the local memory.

We note that this operation is claimed by Appellants. For example, in claim 39, Appellants claim

> said main cache controller and said receive cache controller both further responding to a common memory read request initiated by said instruction processor unit for second data held in said local memory so as to read the second data requested by the read request from one cache which holds said second data among said main cache and said receive cache.

In the only other independent claim, claim 53, Appellants claim

> means responsive to a memory read request provided from the processing unit for read out of second data from said local memory for reading out the second data requested by the memory read request from one of the first and the second cache memories if said one cache memory holds the requested second data and for supplying the read second data to said processing unit.

On page 5 of the answer, the Examiner states that Watkins does not expressly teach the common memory read request to both the central cache and the I/O cache as claimed

by Appellants. However, the Examiner does point us to Segers and

shows that Segers teaches a computer system which comprises a central processing unit (10) and a cache memory system (24) having a primary cache (26) and a second cache (28), wherein the central processing unit (10) sends out a read request to the cache memory system (24). The cache memory system (24) determines whether there is a hit in the primary cache or the secondary cache in a parallel operation. The Examiner points to column 3, lines 57 through 60, and column 4, lines 10 through 13. The Examiner argues that it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the common memory request to both the central cache and the I/O cache in Watkins in view of Segers because Segers teaches that this would improve system performance.

Appellants argue on pages 18 through 20 of the brief that the Examiner improperly modified Watkins in view of

Segers. Appellants argue that the modification proposed by the Examiner is expressly prohibited by the Watkins system. Appellants argue that the entirety of the Watkins disclosure is directed to specialized hardware and software improvements in computer systems that function to control data movements between external devices and main memory. In particular, Watkins is concerned

with the problem of maintaining data consistency between the I/O cache and the CPU cache, which is collectively called consistency controls. Appellants argue that it is improper under 35 U.S.C. § 103 to ignore the invention set forth by the primary reference in order to support a purported obvious modification of the reference in order to meet the claimed invention. Appellants further emphasize this point in the reply brief. In particular, Appellants argue on page 2 of the reply brief that it is not obvious to modify Watkins to form a function specifically prohibited by the system and that the present invention is directed to parallel or multiprocessing systems unlike that of Watkins.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). In addition, the Federal Circuit reasons in ***Para-Ordnance***, 73 F.3d at 1088-89, 37 USPQ2d at 1239-40, that for the determination of obviousness, the court

must answer whether one of ordinary skill in the art who sets out to solve the problem and who had before him in his workshop the prior art, would have been reasonably expected to use the solution that is claimed by the Appellants.

Upon our careful review of Watkins, we find that Watkins is concerned with various data management actions such that when taken ensure data coherency. Watkins teaches that there is a problem in maintaining data consistency between the I/O cache and the central cache. See column 1, lines 32

through 43. Watkins discloses in column 2, lines 29 through 39, that their invention solves this problem of maintaining data consistency between an I/O cache and a CPU cache by a unique combination of hardware and software supports called collectively consistency controls. Watkins further lays out data consistency requirements and operating system consistency guidelines in column 4, line 40, through column 6, line 11. These guidelines make it clear that the CPU is not allowed to access the I/O cache.

Segers is not concerned with the problem of data coherency for an I/O cache. Segers teaches a central processing

unit (10) having a cache memory system (24). The cache memory system (24) includes a primary cache (26) and a secondary cache (28). Segers discloses that the primary cache (26) has a faster access than the secondary cache (28). In column 2, lines 1 through 35, Segers discloses that they are attempting to solve the problem of the time it takes for a cache system

to operate. Segers discloses that the secondary cache memory is configured with Dynamic Random Access Memory (DRAM) and the primary cache memory is configured with Static Random Access Memory (SRAM). The DRAM arrays allow for higher density but sacrifice speed, while the SRAMs have faster access speed but sacrifice density. Segers takes advantage of both of these by providing one cache made up of DRAMs and the other cache made up with SRAMs. However, Segers is not concerned with data coherency between an I/O cache and a main memory cache.

In viewing Watkins and Segers, we fail to find that the prior art suggests the desirability of modifying the Watkins reference so as to destroy the data coherency by allowing the CPU to access both the I/O cache and the main memory cache simultaneously. Therefore, we will not sustain the Examiner's rejection of Appellants' claims under 35 U.S.C. § 103.

In view of the foregoing, we reverse the Examiner's decision rejecting claims 39 through 44, 46 through 51, 53 through 74 and 78 under 35 U.S.C. § 103 as being unpatentable over Watkins, in view of Segers.

REVERSED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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) BOARD OF PATENT
MICHAEL R. FLEMING) APPEALS AND
Administrative Patent Judge) INTERFERENCES
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STUART N. HECKER)
Administrative Patent Judge)

MRF:psb

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Fay Sharpe, Beall, Fagan, Minnich & McKee
104 East Hume Avenue
Alexandria, VA 22301